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Built in Self Test a New Test Generation Pattern

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Abstract: VLSI Chips have some complexity. The increasing level of integration results in small features size, and high proximity of functional units. This leads the system highly susceptible to external faults which turns the need for testing. This paper proposes a Test Pattern Generator for Built-In Self-Test. Our method generates multiple single input change vectors in a pattern, i.e., each vector applied to a scan chain is a SIC vector. A Reconfigurable Johnson Counter and a Scalable SIC counter are developed to generate a class of minimum transition sequences. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. A theory is also developed to represent and analyse the sequences and to extract a class of MSIC sequences. . Analysis results show that the produced MSIC sequences have the favourable features of uniform distribution and low input transition density. It also achieves the system fault coverage without increasing the test length.

Keywords: SIC, TPG, MSIC.

I. INTRODUCTION

1.1 OVERVIEW OF BIST

A Built-in Self-Test or Built-in Test is a mechanism that permits a machine to test itself. BIST is a design-for-testability technique that places the testing functions physically with the circuit under test. The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyser, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register. A typical response analyser is a comparator with stored responses or an LFSR used as a signature analyser. It compacts and analyses the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyse the responses. However, in general, several test-related functions can be executed through a test controller circuit.

A digital system is tested and diagnosed during its lifetime on numerous occasions. Such a test and diagnosis should be quick and have very high fault coverage. One way to ensure this is to specify such a testing to as one of the system functions, so now it is called Built In Self-Test. With properly designed BIST, the cost of added test hardware will be more than balanced by the benefits in terms of reliability and reduced maintenance cost. For BIST, we would require that the test patterns be generated on the system/chip itself. However, this should be done keeping in mind that the additional hardware is minimized. One extreme is to use exhaustive testing using a counter and storing the results for each fault simulation at a place on the chip (like ROM). An n input circuit would then require 2^n combinations which can be very tiresome on the system with respect to the space and the time. Also, more the number of transitions, the power consumed will be more time.

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application can severely decrease the reliability of circuits under test. This is even more severe in circuits equipped with bist, since such circuits may be tested frequently

2. LFSR AS TPG

Linear-Feedback Shift Register is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is XOR. Thus, an LFSR is most often a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle. Linear

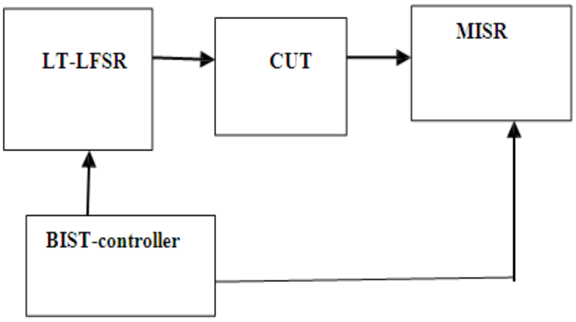


Fig. 1.1 A basic BIST Architecture

The seriousness of excessive power dissipation during test application is exacerbated by trends such as circuit miniaturization for portability and high performance (smaller chips can be placed closer, decreasing interconnect delays). these objectives are typically achieved by using circuit designs that decrease power dissipation and reducing the package size to aggressively match the average power dissipation during the circuit's normal operation. in order to ensure non-destructive testing of such a circuit, it is necessary to either apply test vectors that cause switching activity that is comparable to that during normal circuit operation or remove any excessive heat generated during test using applied at higher special cooling equipment. The use of special cooling equipment to remove excessive heat dissipated during test application becomes increasingly difficult and costly as tests are levels of circuit integration, such as bist at board and system levels. Since temperature and current density are major factors that determine electro migration rate, elevated temperature and current density caused by excessive switching activity during test Feedback Shift Register is commonly used as a test pattern generator in low overhead Built-In Self-Test. This is due to the fact that an LFSR can be built with little area overhead and used not only as a TPG, which provides high fault coverage for a large class of circuits, but also as an output response analyser.

3. LOW SWITCHING OF DS-LFSR

A BIST TPG, which can reduce switching activity during test application, is proposed. The reduction in switching activity is achieved by lowering the transition densities at selected inputs. The proposed TPG, called DS-LFSR, consists of two LFSRs, a slow LFSR and a normal-speed LFSR. The slow LFSR is driven by a slow clock whose speed is $(1/d)^{th}$ that of the normal clock that drives the normal-speed LFSR, thereby, densities at inputs driven by the slow LFSR. The DS-LFSR is designed in such a way that the generated patterns are all unique and uniformly distributed to achieve high fault coverage. The empirical analysis using tests demonstrates that the DS-LFSR generated sequences are more uniformly distributed than the sequences generated by single LFSRs with primitive feedback polynomials. The inputs to be driven by the slow LFSR are selected using a gain function whose value is computed for all inputs.

3.1 Challenges in LFSR

Power dissipation is a challenging problem for today's System-On-Chips design and test. In general, the power dissipation of a system in test mode is more than in normal mode. Four reasons are blamed for power increase during test. They are:

High-switching activity due to nature of test patterns,
Parallel activation of internal cores during test,
Power consumed by extra design-for-test circuitry, and
Low correlation among test vectors.

This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Solutions that are commonly applied to alleviate the excessive power problem during test include reducing frequency and test partitioning/scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time.

Built-In Self-Test is a DFT methodology that aims at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as at-speed testing and reduced need for expensive external automatic test equipment. In BIST, a linear feedback shift register generates pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit). On the observation side, a multiple input signature register compacts test responses received from primary outputs or scan chain outputs. Unfortunately, BIST-based structures are very vulnerable to high-power consumption during test. Test vectors, applied to a circuit under test at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern.

4. CONTRIBUTION OF OUR METHOD

Our method presents the theory and application of a class of minimum transition sequences. The proposed method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. The advantages of the proposed sequence can be summarized as follows,

4.1 Minimum transitions

In the proposed pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power.

4.2 Uniqueness of patterns

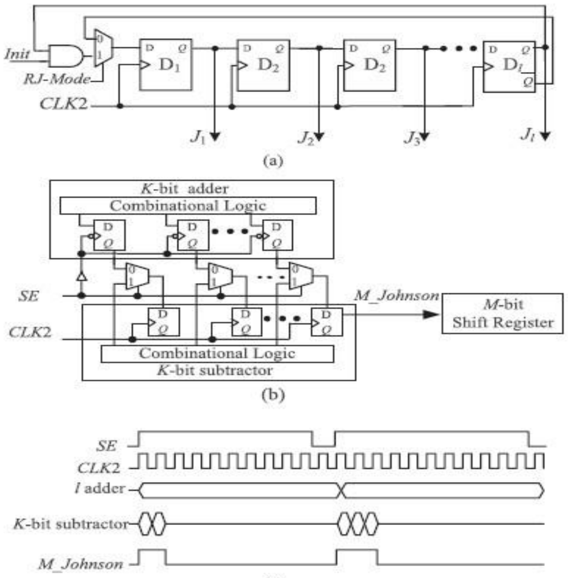
The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequence can meet the requirement of the target fault coverage for the CUT.

4.3 Uniform distribution of patterns

The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time. It is proved in this paper that our Multiple SIC sequence is nearly uniformly distributed.

4.4 Low hardware overhead consumed by extra TPGs

The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a sequential decompressor. Hence, the proposed TPG can be easily implemented by hardware.



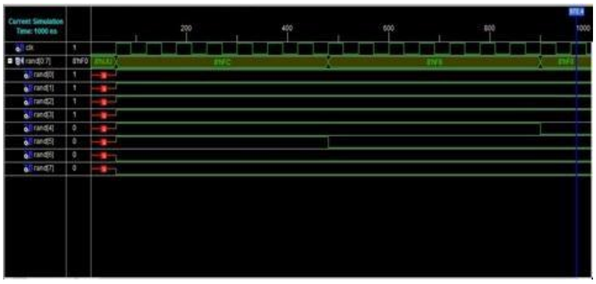
(a)

(b)

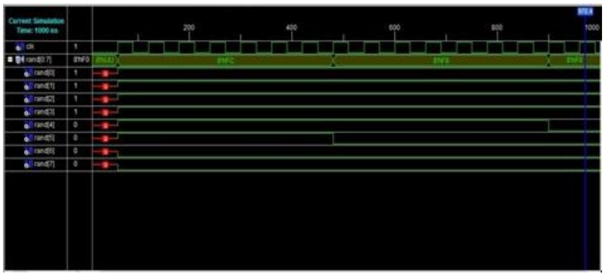
(c)

SIMULATION AND RESULT

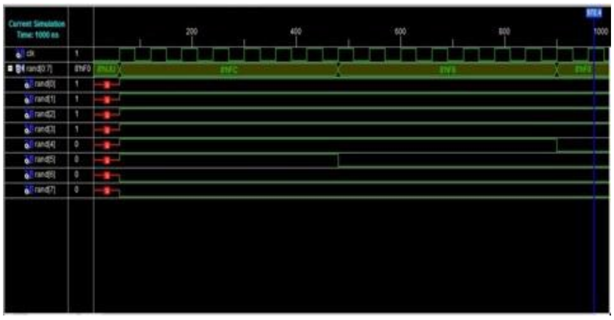
Simulation for LFSR



Simulation for reconfigurable Johnson Counter



RESULT AND ANALYSIS Simulation result for SIC vector



5. CONCLUSION

The proposed method is a low-power test pattern generation method that could be easily implemented by hardware. Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and is flexible to test-per-clock schemes and test-per-scan schemes. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and has negligible impact on the test overhead.

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BIOGRAPHY

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